Program

May 8, 2017

08:15-08:30 Registration

08:30-08:45 Opening

- *Said Hamdioui (General Chair BELAS 2017, Delft University of Technology, the Netherlands)*

08:45-09:45 Keynote: Challenges in IC Design for Automotive (Test, Reliability, Security, ..)

- *Jos van Beers (NXP, the Netherlands)*

09:45-10:45 Coffee break + PhD Forum

10:45-11:30 Tutorial 1: Testing for better Quality and Relaibility: Combining Structural and Functional Test Across System Levels (index.php?id=2215#tutorial_1)

- *Matteo Sonza Reorda (Politechnico di Torino, Italy)*

11:30-11:45 Coffee break

11:45-12:30 Tutorial 1:Testing for better Quality and Relaibility: Combining Structural and Functional Test Across System Levels (index.php?id=2215#tutorial_1)

- *Matteo Sonza Reorda (Politechnico di Torino, Italy)*

12:30-14:00 Lunch

14:00-14:45 Tutorial 2: Manufacturing Defects as Reliability Concerns in SRAMs (index.php?id=2215#tutorial_2)

- *Letícia Bolzani Poehls (PUCRS, Brazil)*

14:45-16:00 Coffee break

16:00-16:45 Tutorial 2: Manufacturing Defects as Reliability Concerns in SRAMs (index.php?id=2215#tutorial_2)

- *Letícia Bolzani Poehls (PUCRS, Brazil)*

16:45-17:30 Coffee break + PhD Forum

19:00-20:30 Dinner

May 9, 2017

08:30-09:15 Tutorial 3: Radiation, Interference and Soft Errors (index.php?id=2215#tutorial_3)

- *Fabian Vargas (PUCRS, Brazil)*

09:15-09:30 Coffee break

09:30-10:15 Tutorial 4: Using Radiant Resilient Programmable SoC devices in Aerospace Applications (index.php?id=2215#tutorial_4)

- *Fernanda Lima Kastensmidt (UFRGS, Brazil)*

10:15-10:45 Coffee break

10:45-11:30 Tutorial 4: Using Radiant Resilient Programmable SoC devices in Aerospace Applications (index.php?id=2215#tutorial_4)

- *Fernanda Lima Kastensmidt (UFRGS, Brazil)*

11:30-11:45 coffee break

11:45-12:30 Tutorial 5: Security in Modern Computer Systems, HW Trojans and SW Vulnerabilities: Threats and Emerging Solutions (index.php?id=2215#tutorial_

- *Fabian Vargas (PUCRS, Brazil)*

12:30-14:00 Lunch

14:00-15:00 Tutorial 6: How to secure the Internet of Things (index.php?id=2215#tutorial_6)

- *Marc Witteman (Riscure, the Netherlands)*

15:45-21:45 Social Event (announce best PhD poster)

- ***15:45-16:15*** *Bus to Delft*
- ***16:15-17:15*** *A guided tour in Delft*
- ***17:15-18:15*** *Boat tour in Delft*
- ***18:15-18:30*** *Walk to Bowling/Restaurant "t Karrewiel*
- ***20:00-21:30*** *Dinner*
- ***19:45-21:15*** *Bowling*
- ***21:30-22:00*** *Bus to hotel*

May 10, 2017

08:30-09:15 Mini-conference Group 1

09:15-09:30 Coffee break

09:30-10:15 Mini-conference Group 2

10:15-10:45 Coffee break

10:45-11:30 Mini-conference Group 3

11:30-11:45 Coffee break

11:45-12:30 Mini-conference Group 4

12:30-12:40 Closing session (announce best perfmorming group)

- *Said Hamdioui (General Chair BELAS 2017, Delft University of Technology, the Netherlands)*

12:40-14:00 Lunch

Detailed Program

TUTORIAL 2

Title: Manufacturing Defects as Reliability Concerns in SRAMs
Speaker: *Letícia Bolzani Poehls (PUCRS, Brazil)*

Abstract: The susceptibility to Single-Event Upsets (SEUs) and aging effects has been treated as the main concerns for Static Random Access Memories (SRAMs) reliability

The role of memory has changed over the last decade; alongside the increasing need to store more and more information, the augmented density has resulted in the fa SRAMs occupy great part of Systems-on-Chip (SoCs). This evolution and miniaturization of technology have brought many changes to semiconductor production. Consequ manufacturing defects may cause static and dynamic faults, which affect the Integrated Circuit's reliability and cause yield loss. Hitherto, the detection of static faults has resolved satisfyingly, while dynamic faults may escape normal manufacturing tests as they do not propagate as faulty behaviour at functional level. Additional stress up cell may transform this apparently harmless fault into a reliability concern though.

Real life situations, among them those for critical applications such as aviation or space, may accumulate influences with negative effects on the memory cell. Environr noise and/or aging may provide the additional stress to cause the SRAM to present faulty behaviour. Therefore, memory cells affected by weak resistive manufacturing d although not impaired under typical environments, may be more susceptible to Single-Event Upsets (SEUs) as well as to aging when in field. In this context, it is import consider the particular impact of Electromagnetic Interference (EMI), radiation and Negative Bias Temperature Instability (NBTI) in SRAM cells with weak resistive defect can escape manufacturing test.

Thus, combined analysis is considered crucial to guarantee the reliability of the memory and subsequently the SoC as a whole.

Biography: Leticia Maria Bolzani Poehls graduated in Computer Science at the Federal University of Pelotas (Brazil) in 2001 and in 2004 she received her Master of S Degree in Electrical Engineering at the Pontifical Catholic University of Rio Grande do Sul (Brazil). In 2008 she received her Ph.D. in Computer Engineering from the Polit di Torino (Italy). During her stay in Turin she worked focusing on the development of New Techniques for Highly Reliable Systems-on-Chip. She holds three postdoctoral the first from 2008 in the field of Low Power Design of Integrated Circuits (ICs) at the Politecnico di Torino, the second from 2010 with focus on Electromagnetic Interfe Aware Systems-on-Chip Design at the Pontifical Catholic University of Rio Grande do Sul (Brazil), and the third from the Politecnico di Torino (Italy) achieved in 2013 in th of Emerging Technologies. At the moment she is Associate Professor at the School of Engineering of the Pontifical Catholic University of Rio Grande do Sul and part of the research laboratory, leading the OASiS research group. Her fields of interest include: Fault Tolerance and Testing of Systems-on Chip, Power-, Aging- and Temperature- Integrated Circuits Design and Development of Electronic Design Automation (EDA) tools for optimization of Integrated Circuits, and ultimately emerging technologies. A other activities, she continues to serve as technical committee member in several IEEE-sponsored conferences and is coordinating editor of Journal of Electronic Te Theory and Application (JETTA).

TUTORIAL 3

Title: Radiation, Interference and Soft Errors
Speaker: *Fabian Vargas (PUCRS, Brazil)*

Abstract: Technology scaling, which made electronics accessible and affordable for almost everyone on the globe, has advanced IC and electronics since sixties. Neverth it is well recognized that such scaling has introduced new (and major) reliability challenges to the semiconductor industry. This talk addresses the background mecha impacting reliability of very deep submicron (VDSM) integrated circuits (ICs). Issues like ionizing radiation (Total-Ionizing Dose: TID and Single-Event Effects: SEEs electromagnetic interference (EMI) are presented and their combined effects on the reliability of modern ICs is discussed. Reliability failure mechanisms for radiation, th they are modeled and how they are impacting IC lifetime will be covered. Laboratory test setup and recent results from experimental measurements are described. C design solutions to counteract with TID, SEEs and EMI in VDSM ICs are introduced.

Biography:

TUTORIAL 5

Title: Security in Modern Computer Systems, HW Trojans and SW Vulnerabilities: Threats and Emerging Solutions
Speaker: *Fabian Vargas (PUCRS, Brazil)*

Abstract: Computer security, also known as cybersecurity or IT security, is the protection of information systems from theft or damage to the hardware, to software a information on them, as well as from disruption of the services they provide. This means that it is mandatory to secure physical access to these systems by protecting against harm that may come via network access, data/code injections and malpractice from operators (designers), whether intentional or accidental. This field is of gr

importance due to the increasing reliance on computer systems and "smart" devices (such as smartphones, smartTVs and tiny devices) as part of the IoT via wireless ne (Bluetooth and Wi-Fi). This talk briefly describes hardware trojans' taxonomy and the most common software vulnerabilities mentioned by specialized literature. C solutions and the cost/benefit to neutralize these threats are also discussed.

Biography:

TUTORIAL 6

Title: How to secure the Internet of Things?
Speaker: *Marc Witteman (Riscure, the Netherlands)*

Abstract: In this tutorial we focus on the protection of IoT against security threats. While this technology is rapidly introduced, there is still much progress to be made in security. We start by sketching the scene and look at the variety of products that we call IoT. Next we show some attacks, and then explain how these relate to long known security threats. We will show why hardware security is vital to IoT, and dive into the specifics of hardware attacks. Finally we explain strateg mitigate hardware attacks and how this is adopted by mature industries.

Biography: Marc Witteman has a long track record in the security industry. He has been involved with a variety of security projects for over two decades and work applications in mobile communications, payment industry, identification, and pay television. Recent work includes secure programming and mobile payment security i He has authored several articles on smart card and embedded device security issues. Further, he has extensive experience as a trainer, lecturing security topics for aud ranging from novices to experts.

As a security analyst he developed several tools for testing software and hardware security. This includes Inspector, a platform for conducting side-channel analys JCworkBench, a logical test tool. Marc Witteman has an MSc in Electrical Engineering from the Delft University of Technology in the Netherlands. From 1989 till 2001 he w for several telecom operators, the ETSI standardization body and a security evaluation facility. In 2001 he founded Riscure, a security lab based in the Netherlands. R offers test tools and services to manufacturers and issuers of advanced security technology. Between 2001 and 2009 he raised the company to a leading security test la side channel test tool vendor. In 2010 Marc Witteman started Riscure Inc, the US branch of Riscure, based in San Francisco. At present he is the Chief Executive Offi Riscure.