Secondment report

Name: ESR1.3 Nevin GEORGE
IRP title: **HW/SW fault tolerance methods driven by reliability and timing constraints**
From: BTU
To: TUT
Period: April 20th – June 01st, 2019

Activities during the secondment

- **Scope and objectives:**
  - To evaluate integration of existing Timing Error Fault Monitors in conjunction with ESR 2.2 Raphael Segabinazzi Ferreira's (BTU), Operating System modification support in an existing Self Health Aware System on Chip Framework
  - To create and advance a Timing Fault Monitor, for evaluation in an existing Self Health Aware System on Chip Framework
- **Activities**
  - Training on Functional Demonstrator of System Health monitoring Capable Framework
  - Brainstorming on points of addition towards support for Monitoring elements and its benefits
  - Progress Meeting reviews of the same
- **Main results achieved**
  - The addition of monitor support was deemed feasible, however at the expense of a greater development time, owing to its fine granular nature.
  - VHDL implementation of Razor and C-Razor elements completed.

- **Next steps.**
  - Owing to the engineering complexity the integration of the components is pending.
  - Evaluation on switching current processor core to better facilitate addition of fine granular Fault Monitors needed.
- **Optional request for support or a technology/tool available at host:**
  - Support request was provided, especially in terms of functional demonstrator training.

Self-evaluation

Overall score: 5
I consider this secondment highly successful, with regards to the research objectives achieved, skills developed, supervision quality, diversity of the resources. (Agree = 5 … Disagree = 1)

Optional comments:
Dr. Artur Jutman's research group, Smart Hardware Research Center (SHARC), at TUT, Tallinn had already an established project in System health awareness with System on Chip. My research interests of adding fault monitors to enhance self-awareness of health and reliability of the system (with a focus on timing errors) therefore was an interesting point of collaboration. Specifically, in understanding the behavior and impact on the aforementioned project's functional demonstrator. The engineering complexity of the functional demonstrator itself was of a higher magnitude owing to lines of code for the RTL description of the processor core and its corresponding system level integration. It must be stated that the integration and experimentation with the fault monitors are still in a continuous phase of development and evaluation.

Date of the report approval by the supervisor: Approved on 7th November, 2019

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